WHAT IS CLAIMED IS:

1. In a processor with an n-way associative cache, a method for prefetching data to the cache comprising the steps of:

issuing a prefetch instruction, wherein said prefetch instruction includes a hint field and address information;

addressing the cache using said address information contained in said prefetch instruction;

indicating a cache miss for said data addressed by said prefetch instruction;

specifying a refill destination for said data in a first portion of said hint field, wherein said destination is a first way in said cache; and

refilling said cache.

2. The method of claim 1 further comprising the step of enabling said specifying step using a second portion of said hint field.

3. The method of claim 2 wherein said refilling step refills said first way of said cache.

4. The method of claim 1 further comprising the step of disabling said specifying step using a second portion of said hint field.

5. The method of claim 4 further comprising the step of refilling a second way of said cache based on a least-recently-used protocol.

6. A processor comprising:

a decoder for decoding a prefetch instruction, wherein said prefetch instruction includes a hint field and address information;

a first n-way set-associative cache, coupled to said decoder, containing a first-cache line that is addressed using said address information;

a first comparator means, coupled to said first cache, for indicating a first-cache miss when said first-cache line is addressed and does not contain desired data; and

a first selection means, coupled to said first cache, for choosing a destination indicator for refilling said first-cache line with said desired data based on a first portion of said hint field.

7. The processor of claim 6 wherein said destination indicator is a second portion of said hint field.

8. The processor of claim 6 wherein said destination indicator is an LRU bit.

9. The processor of claim 7 wherein said second portion of said hint field points to a first way of said first cache, wherein said first way contains streamed data.

10. The processor of claim 7 wherein said second portion of said hint field points to a second way of said first cache, wherein said second way contains retained data.

11. The processor of claim 9 further comprising a means for disabling a refill operation of said cache line when said first way is unavailable.

12. The processor of claim 6 further comprising:

a second n-way set-associative cache, coupled to said first cache, containing a second cache line that is addressed using said address information;

a second comparator means, coupled to said second cache, for indicating a second-cache miss when said second cache line is addressed; and

a second selection means, coupled to said second cache, for choosing said destination indicator for refilling said second cache line based on said first portion of said hint field.

13. A processor comprising:

a decoder for decoding a prefetch instruction, said prefetch instruction including a hint field and being used to refill desired data to a first n-way associative cache; and

a first multiplexer, coupled to said decoder, for choosing a destination indicator based on a first portion of said hint field, said destination indicator being used to direct refilling of said first cache with said desired data.

14. The processor of claim 13 wherein said destination indicator is a second portion of said hint field.

15. The processor of claim 13 wherein said destination indicator is an LRU bit.

16. The processor of claim 14 wherein said second portion of said hint field points to a first way of said first cache, wherein said first way contains streamed data.

17. The processor of claim 14 wherein said second portion of said hint field points to a second way of said first cache, wherein said second way contains retained data.

18. The processor of claim 13 further comprising:

a second multiplexer, coupled to said decoder, for choosing said destination indicator based on said first portion of said hint field, said destination indicator being used to direct refilling of a second cache with said desired data.

19. The processor of claim 13 wherein said destination indicator is a randomly generated bit.